

Phase Control Thyristor

ISOPLUS220™

Electrically Isolated Back Surface

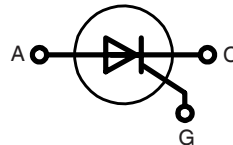
Preliminary Data Sheet

$$V_{RRM} = 800/1200 \text{ V}$$

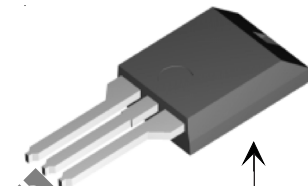
$$I_{T(RMS)} = 35 \text{ A}$$

$$I_{T(AV)M} = 23 \text{ A}$$

V_{RSM} V_{DSM} V	V_{RRM} V_{DRM} V	Type
800	800	CS 29-08io1C
1200	1200	CS 29-12io1C



ISOPLUS 220™



Isolated back surface*

Symbol	Conditions	Maximum Ratings	
$I_{T(RMS)}$	$T_{VJ} = T_{VJM}$	35	A
$I_{T(AV)M}$	$T_C = 95^\circ\text{C}$; 180° sine ($I_{T(RMS)}$ current limit)	23	A
I_{TSM}	$T_{VJ} = 45^\circ\text{C}$; $V_R = 0 \text{ V}$	$t = 10 \text{ ms}$ (50 Hz), sine	200 A
		$t = 8.3 \text{ ms}$ (60 Hz), sine	215 A
	$T_{VJ} = T_{VJM}$; $V_R = 0 \text{ V}$	$t = 10 \text{ ms}$ (50 Hz), sine	175 A
		$t = 8.3 \text{ ms}$ (60 Hz), sine	185 A
I^2t	$T_{VJ} = 45^\circ\text{C}$; $V_R = 0 \text{ V}$	$t = 10 \text{ ms}$ (50 Hz), sine	200 A ² s
		$t = 8.3 \text{ ms}$ (60 Hz), sine	195 A ² s
	$T_{VJ} = T_{VJM}$; $V_R = 0 \text{ V}$	$t = 10 \text{ ms}$ (50 Hz), sine	155 A ² s
		$t = 8.3 \text{ ms}$ (60 Hz), sine	145 A ² s
$(di/dt)_{cr}$	$T_{VJ} = T_{VJM}$; $f = 50 \text{ Hz}$; $t_p = 200 \mu\text{s}$; $V_D = 2/3 V_{DRM}$; $I_G = 0.2 \text{ A}$; $di_G/dt = 0.2 \text{ A}/\mu\text{s}$	repetitive, $I_T = 40 \text{ A}$	150 A/ μs
		non repetitive, $I_T = I_{T(AV)M}$	500 A/ μs
$(dv/dt)_{cr}$	$T_{VJ} = T_{VJM}$; $R_{GK} = \infty$; method 1 (linear voltage rise)	$V_{DR} = 2/3 V_{DRM}$	1000 V/ μs
P_{GM}	$T_{VJ} = T_{VJM}$; $I_T = I_{T(AV)M}$	$t_p = 30 \mu\text{s}$	5 W
P_{GAV}		$t_p = 300 \mu\text{s}$	2.5 W
			0.5 W
V_{RGM}			10 V
T_{VJ}		-40...+150	°C
T_{VJM}		150	°C
T_{stg}		-40...+150	°C
V_{ISOL}	50/60 Hz RMS; $I_{ISOL} \leq 1 \text{ mA}$	2500	V~
T_L	1.6 mm from case; 10 s	260	°C
F_C	Mounting force	11...65 / 2.4...11	N/lb
Weight		2	g

Features

- Silicon chip on Direct-Copper-Bond substrate
- High power dissipation
- Isolated mounting surface
- 2500 V electrical isolation
- Low cathode-to-tab capacitance (15 pF typical)
- Planar passivated chips
- Epoxy meets UL 94V-0
- High performance glass passivated chip
- Long-term stability of leakage current and blocking voltage

Applications

- Motor control
- Power converter
- AC power controller
- Light and temperature control
- SCR for inrush current limiting in power supplies or AC drive

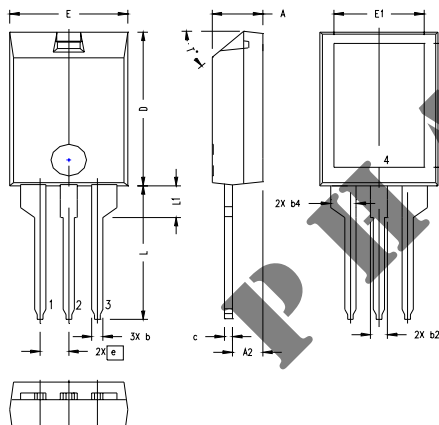
Advantages

- Space and weight savings
- Simple mounting

Symbol	Conditions	Characteristic Values	
I_R, I_D	$T_{VJ} = T_{VJM}; V_R = V_{RRM}; V_D = V_{DRM}$	$\leq$	2 mA
V_T	$I_T = 45 \text{ A}; T_{VJ} = 25^\circ\text{C}$	$\leq$	1.5 V
V_{T0}	For power-loss calculations only ($T_{VJ} = 125^\circ\text{C}$)	0.82	V
r_T		16.5	m Ω
V_{GT}	$V_D = 6 \text{ V}; T_{VJ} = 25^\circ\text{C}$	$\leq$	1.0 V
	$T_{VJ} = -40^\circ\text{C}$	$\leq$	1.2 V
I_{GT}	$V_D = 6 \text{ V}; T_{VJ} = 25^\circ\text{C}$	$\leq$	65 mA
	$T_{VJ} = -40^\circ\text{C}$	$\leq$	80 mA
V_{GD}	$T_{VJ} = T_{VJM}; V_D = \frac{2}{3} V_{DRM}$	$\leq$	0.2 V
I_{GD}		$\leq$	5 mA
I_L	$T_{VJ} = 25^\circ\text{C}; t_p = 10 \mu\text{s}; I_G = 0.2; di_G/dt = 0.2 \text{ A}/\mu\text{s}$	$\leq$	150 mA
I_H	$T_{VJ} = 25^\circ\text{C}; V_D = 6 \text{ V}; R_{GK} = \infty$	$\leq$	50 mA
t_{gd}	$T_{VJ} = 25^\circ\text{C}; V_D = \frac{1}{2} V_{DRM}; I_G = 0.2 \text{ A}; di_G/dt = 0.2 \text{ A}/\mu\text{s}$	$\leq$	2 μs
R_{thJC}	DC current	1.2	K/W
R_{thCK}	DC current	typical 0.6	K/W
a	Max. acceleration, 50 Hz	50	m/s ²

See CS 30..io1 data sheet for electrical characteristic curves.

ISOPLUS220 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5°	47.5°

NOTE:
 1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
 2. This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.

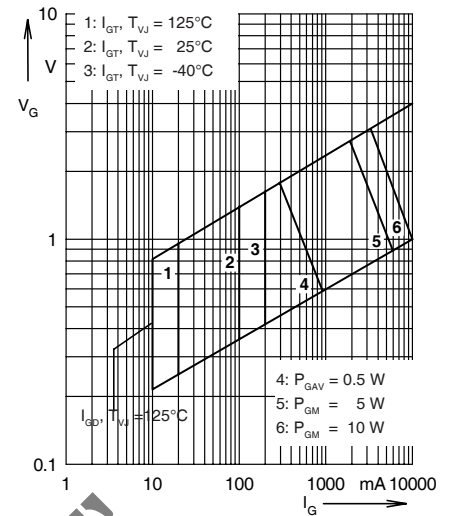


Fig. 1 Gate trigger range

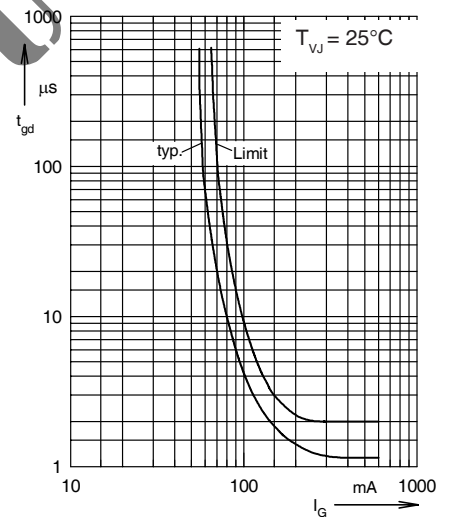


Fig. 2 Gate controlled delay time t_{gd}

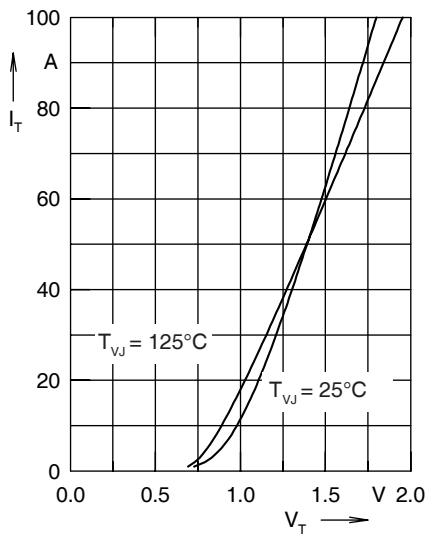


Fig. 3 Forward characteristics

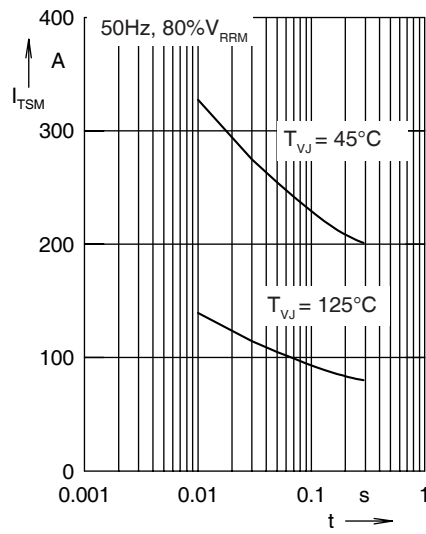


Fig. 4 Surge overload current
 I_{TSM} : crest value, t : duration

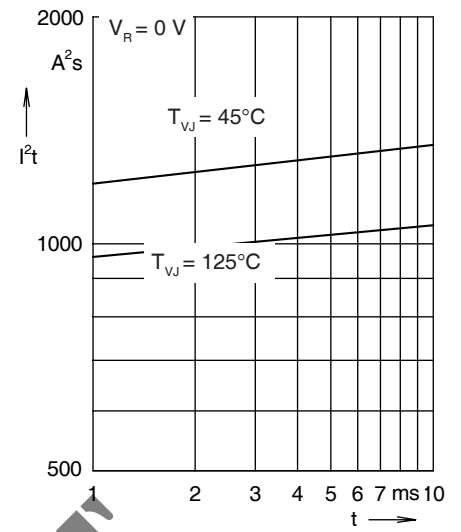


Fig. 5 I^2t versus time (1-10 ms)

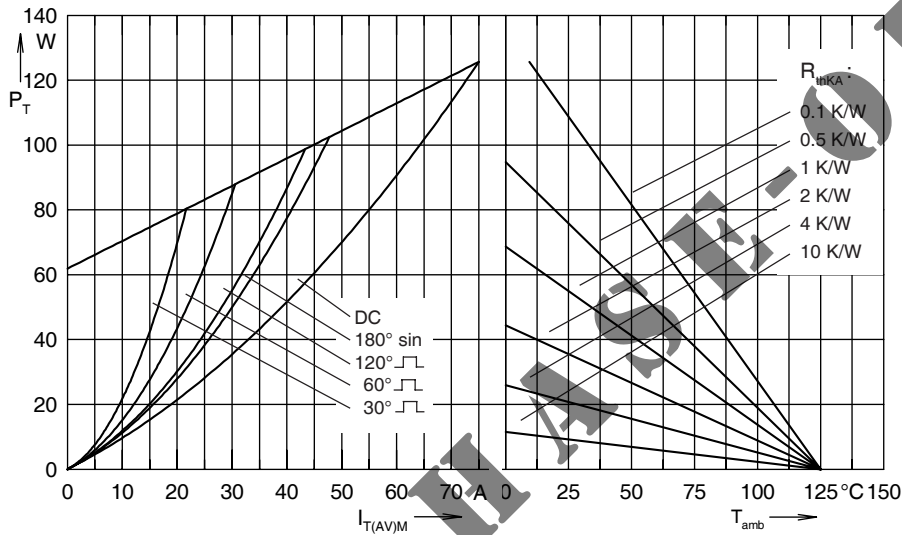


Fig. 6 Power dissipation versus forward current and ambient temperature